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Novel Ultra Low Power Optical Memory using Liquid Crystal

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ABSTRACT

Nowadays, a huge data traffic requires a high-speed processing, so the use of optical memories is a logical solution for high speed data processing. In this paper, a large-scale parallel integration of wavelength addressable optical bit memories is presented based on three photonic crystal nanocavities (C_1, C_2, and C_3) filled with liquid crystal. Each cavity is storing two different wavelengths, where each wavelength is representing a single bit. We have calculated Q factors in basing and unbiasing states for C_1, C_2, and C_3. Also, the group velocities across the storage cell have been measured in the biased and unbiased cases for all cavities to confirm the storage and confinement. The maximum consumed power for six bits optical memory is only 13 nW.

Keywords: Memory, optical RAM, liquid crystal

1. INTRODUCTION

Nowadays many applications require high-speed data processing which can be achieved by using parallel processing computing cores. Unfortunately, the electronic memories and storage do not undergo similar advances and are having drawbacks of bandwidth limitation and long access time. This is imposing major limitation on further enhancing processing capabilities, which is commonly known as Memory Wall [1,2]. This is mainly due to the physical state of electron and transistor technology. Therefore, the optical processing is a logical alternative solution due to its advantage of high-speed transmission.

The photonic integration has been under research for last decade, but the integration level is very limited when compared to that of electronics. The limitation for large-scale integration is mainly due to their large footprint and high consumption power. However, the need for large-scale photonic integration has been highly demanding for the optical processing applications. In the quest for designing and optimizing optical memories, many trails have started in various forms starting from ring lasers disks targeting the design of flip-flops [1-3] to the design of cavities with high-quality factors (Q_f) [4,5].

The main issues for large scale memory integration are power consumption of single cell, bit representation, and footprint. Many researchers have investigated these issues for optimization. Notomi *et.al* have adapted the ideas of optimizing the micro/nano cavities for ultra-low power all optical RAM in full scale integration [4,5]. Nozaki *et al.* have demonstrated the design of optical random access memory (O-RAM) based on 2D Indium phosphide (InP) photonic crystal (PhC) cavity with a buried membrane of Indium gallium arsenide phosphide (InGaAsP) with power consumption

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of 30 nWb^{-1}, switching energy 2.5 fJ with high switching speed (ON: 44 ps , OFF: 7 ns) and storage area of 10 μm^2 for a single bit [4]. The cavity design was based on the waveguide modulation by shifting three rows of air holes in the *y*-axis direction. The operation of O-RAM was depending on the nonlinearity of materials. The reading, writing, and resting operations are controlled by increasing or decreasing the biased power. The area of the design has been optimized for the single bit state but in case of large scale integration it demands a large area as the distance between each bit cell is 50 μm in 4 bits parallel integration and the power consumption is near 1 μW.

As an alternative solution for integrability, Kuramocha *et al.* [5] have demonstrated the capabilities of wavelength addressable O-RAM on a photonic crystal chip. The design concept is to modulate and assign each bit to specific wavelength with 0.9 nm spacing to be stored in series of serial nano-cavities. For storing 28 bits, they have optimized and fabricated 28 cavities with a separation distance of 8.4 μm to have total length of 286 μm with total power consumption of 137 μW. The reported power consumption for single bit is 4.8 μWb^{-1}.

All previous works were depending on the nonlinearity of InP and InGaAsP materials that always fed by optical biasing power for optical operation. The bit representation of binary operation (0s and 1s) were depending on ON and OFF light pulse. As for reading and writing operation for optical memory it was operating by a slight increase or decrease of biasing power fed to optical memory that change Q_f of nanocavity. The most common drawback of all previous memories is the biasing power which leads to high power consumption and lowering dynamicity of switch rate between ON and OFF state in reading and writing process.

In this work, we present a low power parallel integration of wavelength addressable optical bit memories using combination between Photonic crystal and liquid crystal. The proposed memory consists of three photonic crystal (PhC) nanocavities etched in indium phosphide (InP) substrate and filled with 5CB liquid crystal allowing two-bit storage for single cell, where each bit is represented by different wavelength. The proposed design has some advantages over those reported previously in literature [1-5] in terms of in size, operating power, and number of stored bits:

- The design of optical memory footprint is one third of that of designs mentioned in [4,5].
- The maximum consumed power for six bits optical memory is only 13 nW which is less than that proposed in [1-5].
- The proposed optical memory can store six bits on three bits memory footprint.

The proposed design is numerically simulated and analyzed using finite difference time domain (FDTD) [6].

The paper is organized as follows. Following this introduction, a detailed description of the proposed memory and numerical methods will follow in section 2. Section 3 presents the simulation results of the design stages of the memory. Finally, the conclusion of the paper will be presented.

2. DESIGN AND NUMERICAL METHODS

The Photonic crystals have attracted much attentions in various fields such as polarizers [7,8], filters [9], and sensors [10-18]. The proposed design cell is based on 2D photonic crystal etched in InP substrate of size 30.6 μm × 14 μm. The use of InP is inspired from previous work [4,5], where it supports low consumed power device rather than silicon substrate. The design for the 6-bit storage cell consists of two main parts which are three cavities (C_1, C_2 and C_3) and demultiplexer.

The demultiplexer is for the separation of the modulated bits and sending each bit to its storage cell. It is designed by introducing shifted branches of Y- splitter as shown in Fig. 1 where this shift breaks the wavelength symmetry for each branch. As for storage cells, they consist of square holes filled with 5CB liquid crystal of size 850 × 850 nm, three surrounding layers surrounding holes and line 1D PhC.

The Liquid crystals (LCs) are defined as fluids where their electrical permittivity tensor (ε_r) is highly depending on the orientation of their molecules and that it is why it attracts many research for various devices such as storage

devices[19], fibers [20-24], multiplexers [25-28], sensors [29,30], logic gates [31] and routers [32,33]. Equation 1 describe relation between ε_r and the molecule orientation [19-33]:

$$\varepsilon_r = \begin{pmatrix} n_o^2\cos^2\varphi + n_e^2\sin^2\varphi & (n_e^2 - n_o^2)\cos\varphi\sin\varphi & 0 \\ (n_e^2 - n_o^2)\cos\varphi\sin\varphi & n_o^2\sin^2\varphi + n_e^2\cos^2\varphi & 0 \\ 0 & 0 & n_o^2 \end{pmatrix} \quad (1)$$

where φ is the rotation angle of the director of the LC with respect to *y*-axis.

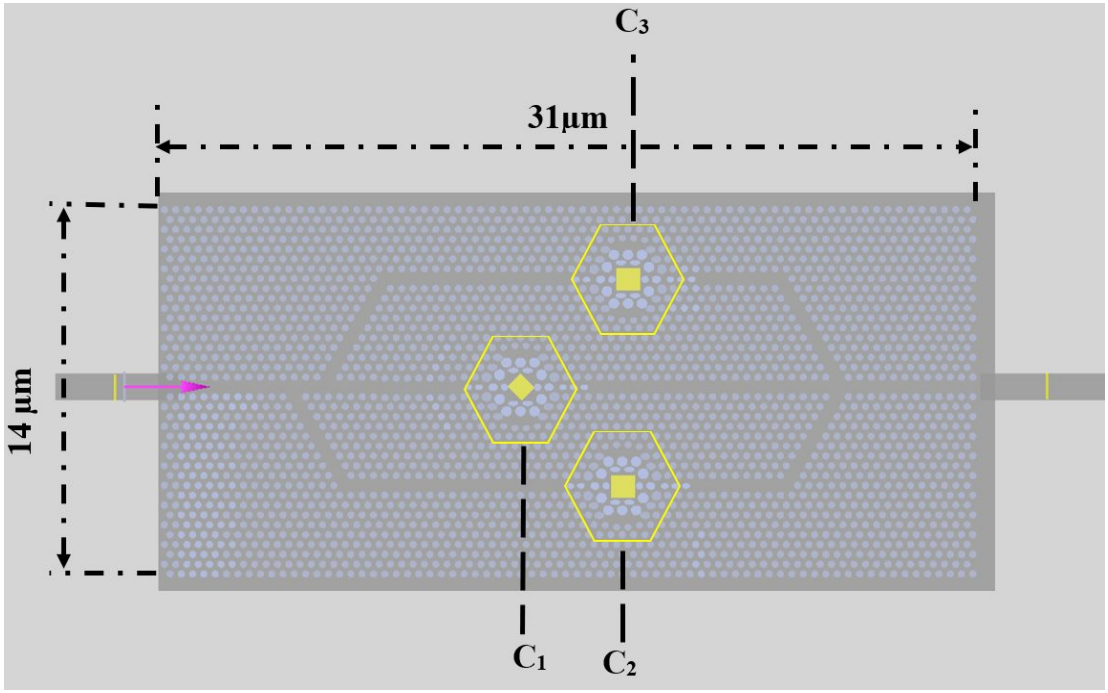


Fig.1. A sematic diagram of proposed design.

The proposed design is simulated using FDTD [6] with simulation window of length equals 33.5 µm and having a width of 14.6 µm which is discretized using an auto non-uniform meshing of minimum mesh step of 0.025 nm. The computational window has been surrounded by the perfect matched layer (PML) boundary conditions [6]. The proposed design is injected with the fundamental mode pulse having wavelength range from 1.4 µm to 1.6 µm in direction of positive x -axis perpendicular to y normal plane.

The Q_f is calculated in both biased state and unbiased state using Q analysis of Lumerical having the expression of [6]:

$$Q_f = \frac{-2\pi f_r \log(e)}{2m} \quad (2)$$

where *m* is the slope of the log of the time signal envelope and f_r is the resonant frequency of the mode.

The Q_f is calculated in both biased state and unbiased state using Eq.2. The biased cases is the case when LC is exposed to electric field; The LC director starts to align parallel to the electric field lines so its rotational angle (φ) changes with the changing of the value of the electric field and this affects the relative permittivity tensor which is responsible for high switching between two bits.

3. SIMULATION RESULTS

The design concept is to change geometry of nanocavities in order to have high Q_f [34-41], with different resonating wavelengths in the presence of liquid crystal. Accordingly, we design PhC cavity to ensure the presence of soft confinement which is a key to achieve a high Q_f. We use a combination of perfect circular and elliptical holes along the coupling waveguide and surrounding holes around LC. The design of storage cell consists of square etching filled with 5CB liquid crystal, two layers surrounding holes and line 1D PhC.

The design cell is based on 2D photonic crystal of air holes having radii *r* = 135 nm with lattice constant in direction of x axis (a_x) equals 425 nm and lattice constant in y axis (a_y) equals 368 nm are etched in InP slab resulting in having a band gap of 370 nm centered at 1600 nm as shown in Fig 2.

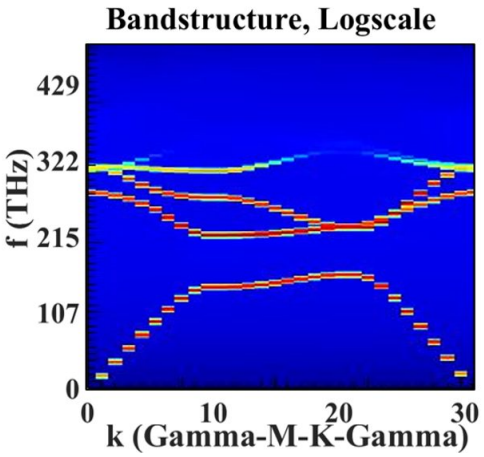


Fig.2 The proposed PhC bandgap with *a* = 425 nm and *r* = 135 nm.

We first optimize the dimension of 1D PhC for the single stored cell then start to optimize the other cell elements in the three cavities design. The first design step for storage cell is 1D cavity. The importance of 1D cavity is to ensure two basic functions which are the soft confinement inside the LC cell and to ease the coupling between the waveguide and storage cell [41]. As shown in Fig. 3(a), the air holes have lattice constant (a_x) of 425 nm with radii of r_y^{1D} and r_x^{1D} along y-axis and x-axis respectively. The air hole geometrical parameters are optimized in order to achieve highest Q_f in biased case of LC and nearly half its value in unbiased case. The radii that apply the optimizing condition is 0.25 a_x and 0.4 a_y to have Q_f of 80000 and 56400 for biased and unbiased case respectively as in Fig. 3(b) and Fig. 3(c). The Q_f increased more than six times than that in absence 1D PhC owing to the presences of elliptical holes that increase the group index of the design this is due to the sharp changing in refractive index of minor axis of elliptical holes [41].

Based on the Q_f calculation in the 1D PhC cavity that the shape alteration from the regular circle to ellipse offers a great structural freedom to tune the optical properties of the nanocavities [41] and increase the Q_f . In this stage, we focus on the upper and lower holes that indicated in Fig. 4.a. by the yellow ellipse holes to study the relationship between the Q_f and radii variation in presence of slight shift in their center positions towards the LC by 4.25 nm and 3.68 nm in x-axis and y-axis respectively. In terms of optimizing the geometry of cavity, the radii in x-axis (r_x^1) and y-axis (r_y^1) changes from zero to half value of a_y and a_x as shown in Fig. 4.b and 4.c for both biasing cases. The maximum Q_f is at radii r_y^1 and r_x^1 having values of 0.3 a_y and 0.45 a_x respectively. The Q_f in the biased case is equal to 121500 and in unbiased case equals to 74500.

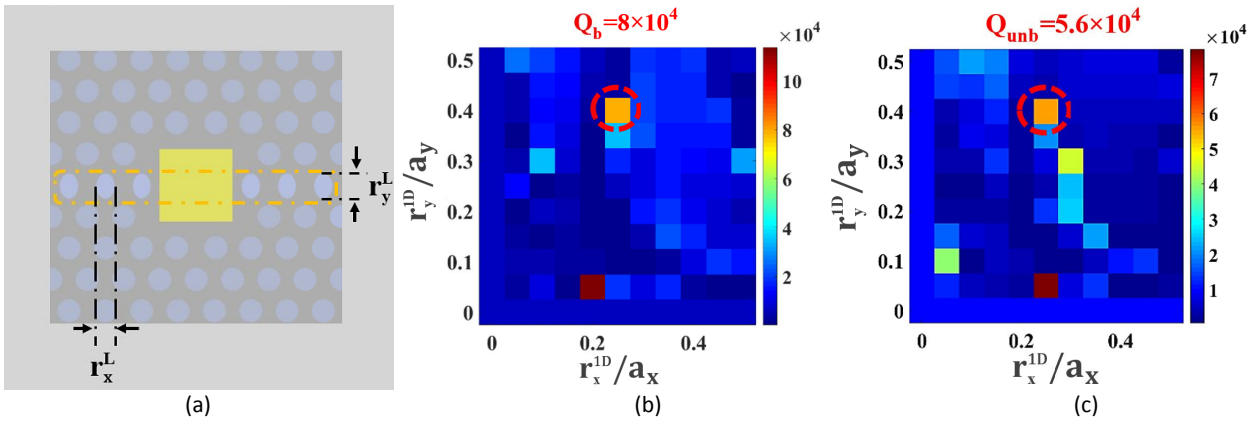


Fig. 3 (a) Design of 1D cavity with liquid crystal inside square etching in InP slab, (b) quality factor as varying ellipse holes radii function of a_x and a_y in biased case, and (c) quality factor as varying ellipse holes radii function of a_x and a_y in unbiased case.

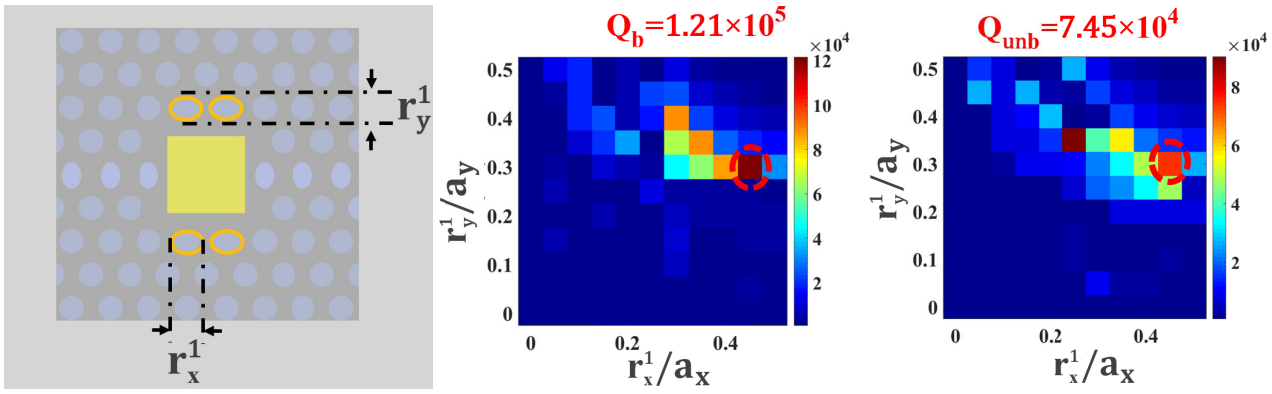
The design of the three storage cells is based on the single storage but with some modifications. These modifications are granting a high-quality factor for six different wavelengths depending on the biasing state of liquid crystal. We have shifted the first and second surrounding holes by 215 nm towards the LC for the adapting the storage cell for new wavelengths. In addition, we have changed the size of second and third surrounding holes as in Fig. 5.a.

In this design stage we are varying the radii of the second surrounding level around the liquid crystal (r_{xy}^2) in three cells (indicating by a yellow hole) as shown in Fig. 5.a to increase Q_f of the cell in biasing and unbiasing state of the liquid crystal. Fig. 5.b shows that the hole radius (r_{xy}^2) is varying from 0 to 200 nm. The optimum r_{xy}^2 is equal to 190 nm having the highest Q_f for C_2 and C_3 in both biasing states as shown in table 1.

Table 1. The Q_f and resonating wavelength (λ) for each cavity in biasing and unbiasing state at r_{xy}^2 equal to 190nm:

Biasing state	C_1		C_2		C_3	
	Q_1	λ_1 (μm)	Q_2	λ_2 (μm)	Q_3	λ_3 (μm)
biased	62000	1.53	523000	1.493	618000	1.484
unbiased	60000	1.52	300000	1.494	364000	1.497

Unfortunately, the Q_f for the C_1 in biased state (Q_{1b}) and unbiased state (Q_{1unb}) are very low if it is compared to that of other cavities which is nearly equal 60000 as demonstrated in Fig. 5.c. Accordingly, we had to try another optimization level to increase the Q_{1b} and Q_{1unb} with keeping the high Q_f of other cavities.



(a) (b) (c)

Fig. 4. (a) The design of 2D cavity with liquid crystal inside square etching in InP slab, (b) quality factor as varying ellipse holes radii function of a_x and a_y in biased case, and (c) quality factor as varying ellipse holes radii function of a_x and a_y in unbiased case.

The Aim from varying the third surrounding level around the liquid crystal in the three cells is to level to increase the Q_{1b} and Q_{1unb} with keeping the high values Q_f of other cavities. The variation of hole radius in (r_x^3) is changing in the *x*-axis and keeping the radius in *y*-axis as its fixed at 135 nm. The r_x^3 equal to 180 nm having the highest Q_f for C_2 and C_3 in both biasing states.

Table 2. The Q_f and resonating wavelength (λ) for each cavity in biasing and unbiasing state at r_x^3 equal to 180 nm :

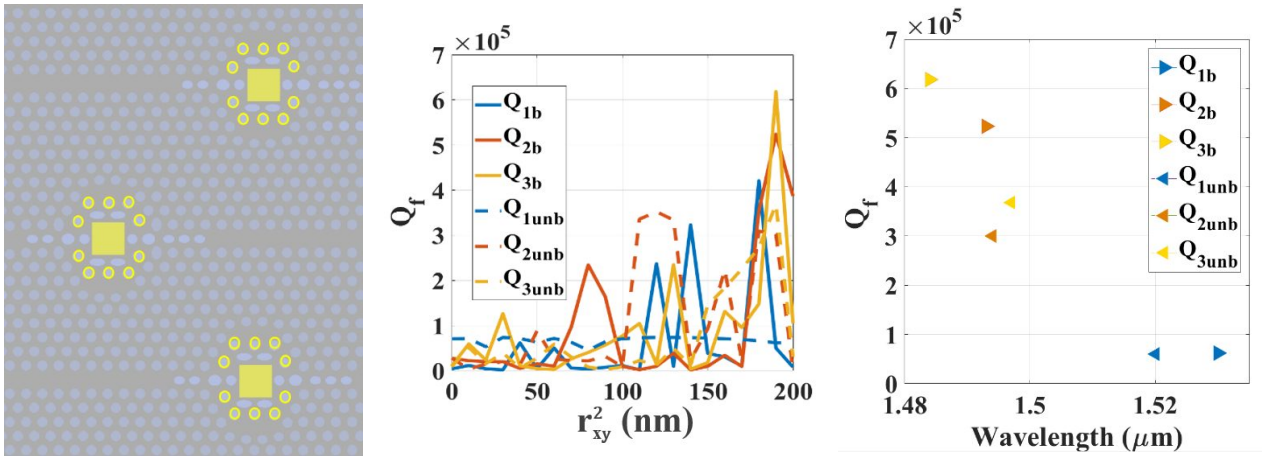
Biasing state	C_1		C_2		C_3	
	Q_1	λ_1 (μm)	Q_2	λ_2 (μm)	Q_3	λ_3 (μm)
biased	63000	1.535	500000	1.493	400000	1.484
unbiased	30000	1.528	300000	1.494	200000	1.497

However, it has the highest difference between Q_{1b} and Q_{1unb} but they are still very low if they are compared to that of other cavities nearly equal 65000 and 30000 for the biased and unbiased states. To increase the Q_{1b} and Q_{1unb} we had to optimize the C_1 only.

Next step is to rotate the liquid crystal inside the C_1 by 45° and changing the dismission of liquid crystal (LC_1 y span) as indicated in Fig. 7.a. The calculated quality factor Q_{1b} and Q_{1unb} are shown in Fig. 7.b. as the *y* span is varying from 750 nm to 1000 nm. The Q_{1b} and Q_{1unb} is nearly doubled at *y* span equals to 750 nm with keeping the values of Q_f of other cavities high as illustrated in table 3.

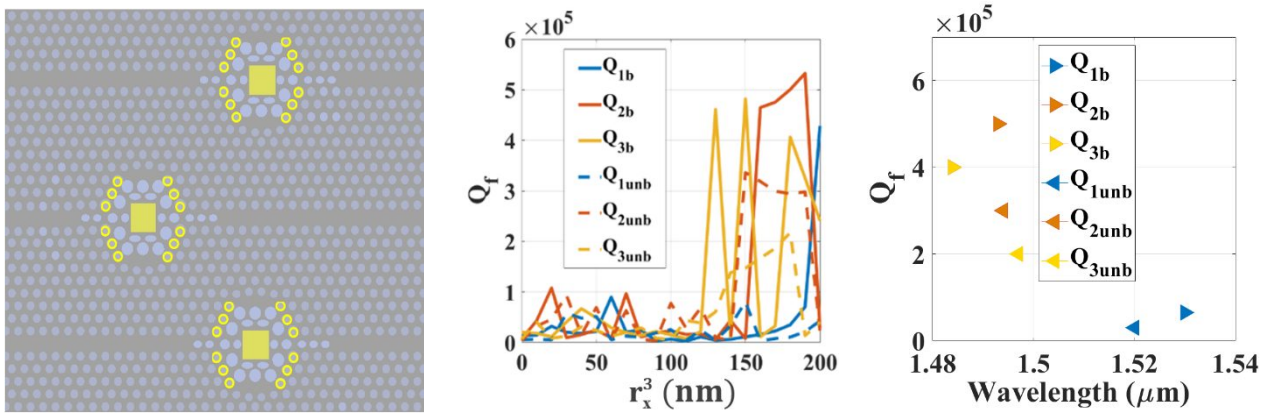
Table 3. The Q_f and resonating wavelength (λ) for each cavity in biasing and unbiasing state at LC_1 y span equals 750 nm:

Biasing state	C_1		C_2		C_3	
	Q_1	λ_1 (μm)	Q_2	λ_2 (μm)	Q_3	λ_3 (μm)
biased	135000	1.528	500000	1.493	400000	1.484
unbiased	90000	1.507	300000	1.494	200000	1.497



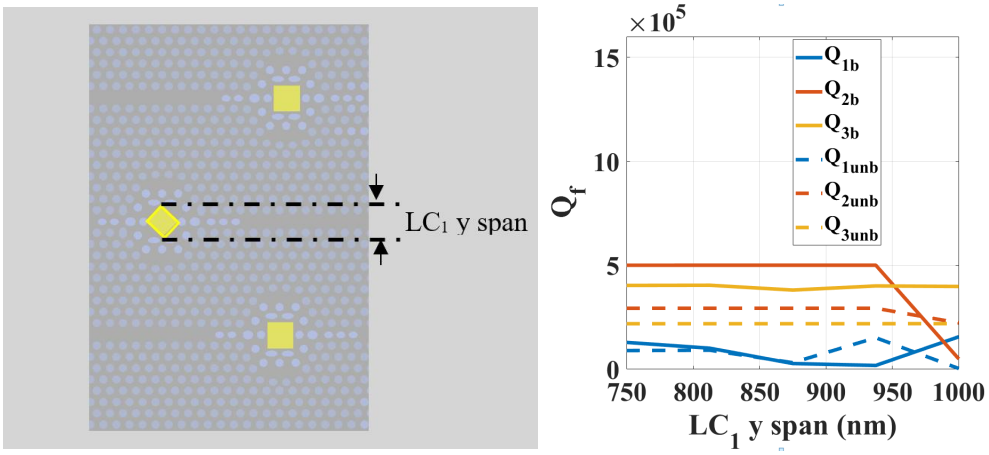
(a) (b) (c)

Fig.5. (a) A schematic diagram of the proposed design with variation of second row radii (r_{xy}^2) indicating to yellow holes, (b) Quality factor variation due to variation of r_{xy}^2 in biasing and unbiasing states, and (c) Quality factor spectrum of the cavities in biasing and unbiasing states.



(a) (b) (c)

Fig.6. (a) The sematic diagram of the proposed design with variation of third row radii (r_x^3) indicating to yellow holes, (b) The quality factor variation due to variation of r_x^3 in biasing and unbiasing states, and (c) The quality factor spectrum of the cavities in biasing and unbiasing states.



(a) (b)

Fig.7. (a) Schematic diagram of proposed design with variation of LC_1 y span and (b) quality factor variation due to variation of LC_1 y span in biasing and unbiasing state.

Another indication for optical trapping is the group velocities across the storage cell. Table 4 shows the calculated group velocities in the biased and unbiased cases for C_1, C_2, and C_3 and normalized to light velocity (V_g/C).

Table 4. The normalized group velocity for each cavity in biasing and unbiasing state:

Biasing state	**V_{g1}/C**	**V_{g3}/C**	**V_{g3}/C**
Biased	-4×10^{-4}	-1.9×10^{-4}	-2×10^{-4}
Unbiased	-5.5×10^{-4}	-4.2×10^{-4}	-3.4×10^{-4}

The negative values can be explained as the transmitted pulse is slowing down and compressed while it propagates along waveguide then coupled inside the cavity and stopped for time frames. The pulse begins to propagate backward after stopping for a while instead of being trapped forever inside the cavity [42]. The small value of the group velocity is owing to the changing and modulating of the surrounding holes resulting in increasing the group index of the cavity to be higher than the average index of liquid crystal [43].

The electric field distribution also confirms the confinement inside the cavities for resonating wavelengths in biasing state and unbiasing states. The field distribution is calculated for C_1, C_2, and C_3 at wavelengths 1.528 µm, 1.493, and 1.484 respectively. Also, it is calculated for the unbiasing state for C_1, C_2, and C_3 at wavelengths 1.507 µm, 1.494, and 1.497 respectively. The field distribution reveals a field confinement within the boundaries of cavities for both biasing cases. In addition, the optical confinement becomes more gradually around the holes, while the electric field distribution decays abruptly outside the holes. This reveals that the stored field inside the cavity in biasing state is double that in unbiasing state as shown in Fig. 8.

One of the most important parameters for estimating the proposed RAM performance is the power calculation. The consumed power in all literature design were more than 3 μWb^{-1} , while the proposed design have maximum estimated power of 13 nW for storing 6 bits.

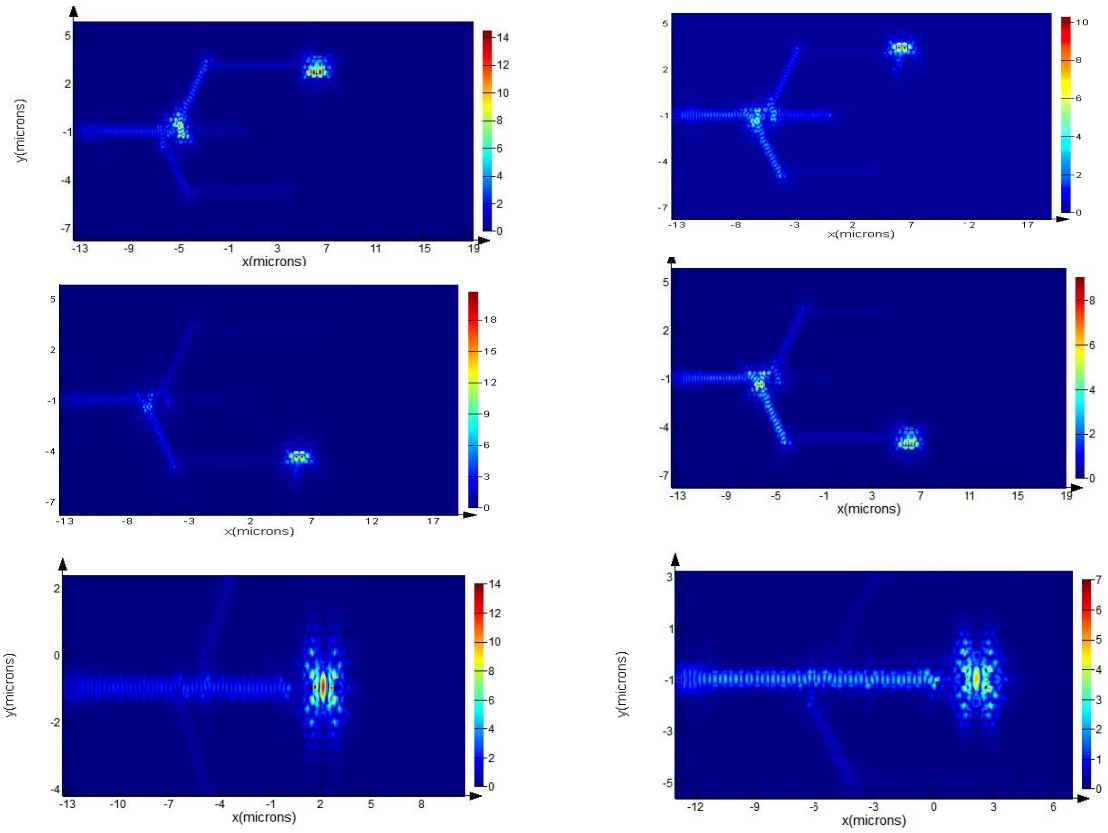


Fig. 8. (a) Electric field distribution for stored field inside the cavity in biased case and (b) electric field distribution for stored field inside the cavity in unbiased case.

Conclusion

In this work we present a low power parallel integration of wavelength addressable optical bit memory based on integration between 2D photonic crystal and 5CB liquid crystal. The suggested design consists of a demultiplexer and three cavities (C_1, C_2, and C_3) with liquid crystals infiltrated inside center of each cavity. We have optimized the dimensions of surrounding holes of each cavity in order to have high quality factor in both biasing and unbiasing states of liquid crystal. We have achieved Q factors in basing states for C_1, C_2, and C_3 equal 1.35×10^5, 4×10^5, and 5×10^5, respectively. Also, the Q_f in the unbiased case is calculated, they have smaller values of 0.9×10^5, 2×10^5, and 3×10^5 respectively. The calculated group velocity and field distribution in both biasing state for liquid crystal are also confirming the confinement of light in the cavities. The consumed power for proposed design is 13 nW which is much lower than that in literature.

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