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Sheet (2) : Analog ICs ELE221
Power Amplifiers

1- For the class B output stage of figure (1) let V_{cc}= 6V and R_L = 4 Ω, if the output is sinusoid with 4.5 V peak amplitude, find :
   a- output power
   b- the average power drawn from each supply
   c- the power efficiency obtained at this output voltage
   d- the peak currents supplied by V_i , assuming that $\beta_N = \beta_p = 50$
   e- the maximum power that each transistor must be capable of dissipating safely

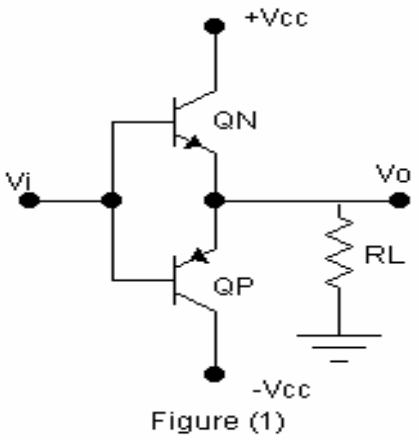

Figure (1)

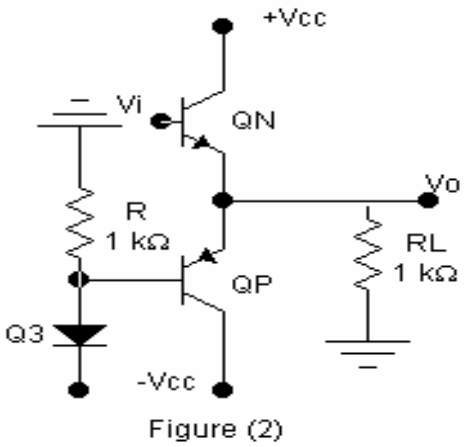

Figure (2)

2- A class A emitter follower, biased using the circuit shown in figure (2), all transistors are identical. Assume V_{BE} = 0.7Vv , V_{CEsat}= 0.3 v, and β very large.

   a) For linear operation, what are the upper and lower limits of output voltage?
   b) and the corresponding inputs?
   c) How do these values change if the emitter base junction area of Q_3 is made twice as big as that of QP? Half as big?

3- A source-follower circuit using enhancement NMOS transistors is constructed following the pattern shown in figure (2). All transistor are identical with V_t=1V and $\mu_n C_{ox} W/L$ = 20 mA/V^2 .
   For linear operation what are the upper and lower limits of the output voltage, and the corresponding inputs?

4- Consider the feedback configuration with class B output shown in figure (3). Let A_o = 100 V/V . Derive an expression for V_o versus V_i assuming that V_{BE} = 0.7V. Sketch the transfer characteristic V_o versus V_i and compare it without feedback.

5- A class AB output stage, resembling that in figure (4) but with supply of +10 V and biased at V_i = 1V, is capacitively coupled to a 100 Ω load. V_{BE} = 0.7V at 1 mA and for bias voltage of V_{BB} = 1.4V. What quisent current results? For a step change in output from 0 to –1 V, what input step is required ? Assuming transistor saturation voltages of zero, find the largest possible positive and negative-going steps at the output.

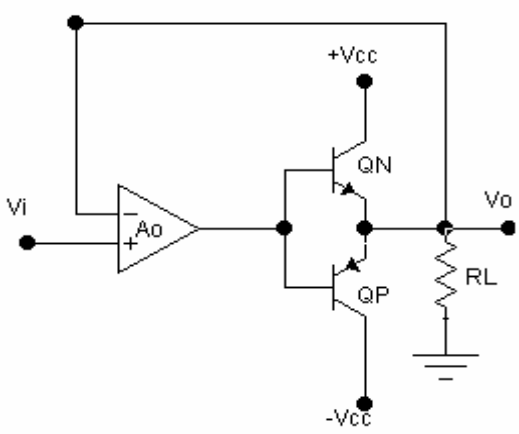

Figure (3)

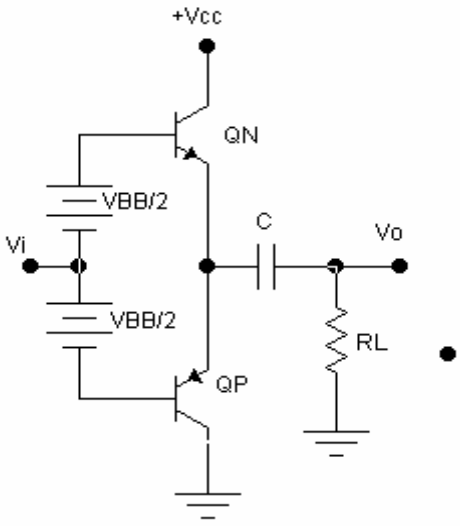

Figure (4)