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Sheet (4) : Analog ICs ELE322
MOS-Differential and BiCMOS Amplifiers

1. Consider the MOS differential pair shown in figure (1) with gate of Q2 grounded. Let $\mu_n C_{ox}$ =20 μ A/V^2, V_t = 1V, W/L = 20, and I = 16 μ A. Find v_{GS1}, v_{GS2}, v_S, and v_{G1} that correspond to the following distributions of the current I between Q_1 and Q_2:
   a- $i_{D1} = i_{D2} = 8\ \mu$ A
   b- $i_{D1} = 12\ \mu$ A and $i_{D2} = 4\ \mu$ A
   c- $i_{D1} = 16\ \mu$ A and $i_{D2} = 0\ \mu$ A (Q_2 is just cuts off.)
   Confirm that the value of v_{G1} obtained in (c) is the same as found using the equation given in lectures.
2. An NMOS differential amplifier utilizes a bias current of 8 μ A . The devices have V_t = 1V, W = 60 μ m, and L = 6 μ m, in a technology for for which $\mu_n C_{ox}$ =20 μ A/V^2. Find V_{GS}, g_m , and the value of v_{id} for full current switching. To what value should the bias current be changed in order to double the value of v_{id} for full current switching.
3. Design the MOS differential amplifier of figure (1) to operate at $V_{GS} - V_t$ = 0.2 V and to provide a transconductance g_m of 0.1 mA/V. Specify the W/L ratios and the bias current. The technology available provides V_t = 1V and $\mu_n C_{ox}$ =20 μ A/V^2.
4. An NMOS differential pair is to be used in an amplifier whose drain resistors are 100 kΩ $\pm$ 1%. For the pair K = 100 μ A/V^2 and V_t = 1V. A decision is to be made concerning the bias current to be used, whether 100 μA or 200 μA. For differential output, contrast the differential gain and input offset voltage for the two possibilities.
5. An NMOS amplifier, whose designed operating point is with V_{GS} one-half volt above the nomimnal 1-V threshold, is suspected to have a viariability of V_t , K, and R_D(indepently) of $\pm 5\%$. What is the worstcase input offset voltage you would excpect to find? What is the major contribution to this total offset? If you used a variation of one of the drain resistors to reduce the output offset to zero and thereby compensate for uncertainties (including that of the other R_D), what percentage change from nominal value would you require? If by selection you reduced the contribution of the worst case of the offset by a factor of 10, what change in R_D would be needed?
6. For the simple MOS mirror shown in figure (2) the devices nominally have K = 100 μ A/V^2 and V_t = 1V. Measurement with $V_{DS2} = V_{DS1}$ and I_{REF} = 1 mA shows the output current to be 5% low. It is assumed that Q_2 differs from Q_1 in one or more ways. If the difference in current is all due to K_2 being different from K_1, find what this difference must be. If, on the other hand, the difference in current is all due to V_{t2} being different from V_{t1}, find what this difference must be.

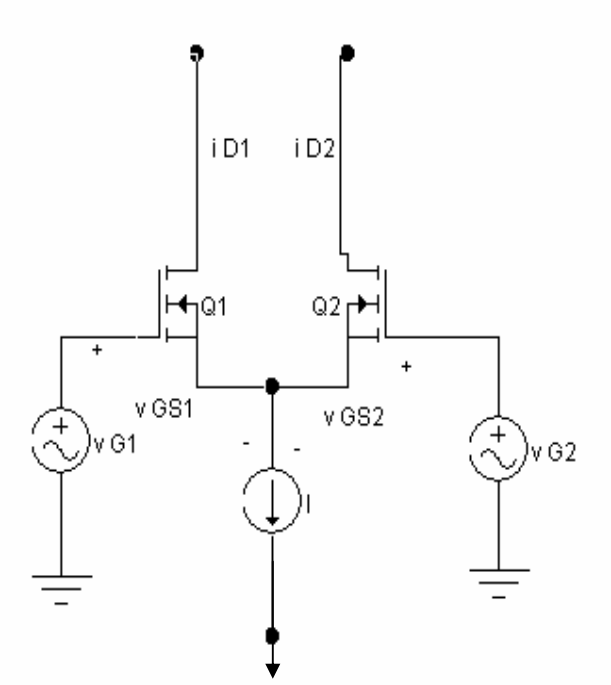

Figure (1)

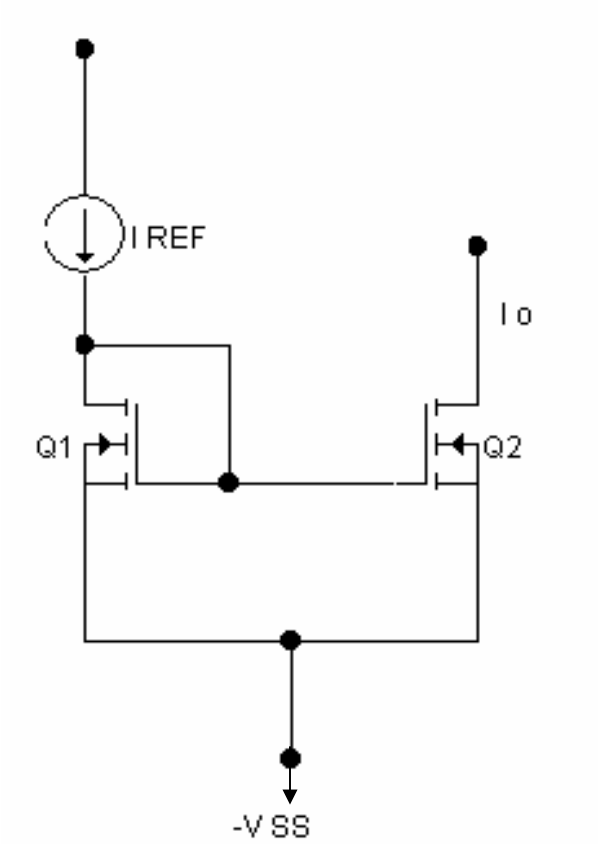

Figure (2)

7 What W/L ratio must a MOSFET have in order to have a g_m equal to that of a BJT when both are biased at a current I of 100 μA. Comment on the results

8 If the parameter λ of a MOSFET is approximately inversely proportional to to the channel length L, how do r_o and the intrinsic voltage gain change with L?

9 How does the thickness of the gate oxide affect the intrinsic gain of the common-source amplifier? Discuss the trade-offs that have to be considered in deciding on oxide thickness?

Hint: If not stated otherwise consider for BJTs: V_A = 50V and β =100; and for MOSFETs: L = 2 μ m, $\lambda = 0.05V^{-1}$, $|V_t|$ = 1 V, and $\mu_n C_{ox}$ =20 μ A/V^2.