Alexandria Institute of Technology
Electronics Section

Course: Digital Integrated Circuits
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Sheet : 2
SAT and SUN

1. An enhancement-load inverter having $(W/L)_1 = 3$ and $(W/L)_2 = 1/3$ is fabricated with a technology for which the minimum practical transistor dimension (length or width) is 5 μm. Find the area occupied by this inverter and the value of its K_R. if K_R is to be quadrupled, find the ration (W/L) for each device so that the silicon area required by the inverter is the minimum possible.

2. Consider an enhancement-load inverter having $V_{t0} = 1$ V, $(W/L)_1 = 3$, $(W/L)2 = 1/3$, $\mu_n C_{OX} = 20\ \mu A/V^2$, $2\Phi_f = 0.6$ V, $\gamma = 0.5\ V^{1/2}$ and $V_{DD} = 5$ V.

   a) Neglecting the body effect, find the critical points of the voltage transfer characteristic, and hence find the noise margins.

   b) Taking the body effect into account, find the modified values of V_{OH} and NM_H.

   c) Find the inverter current in both states, and hence find the average static power dissiption.

3. For the enhancement-load inverter of Fig. 1, find K_R that result in $V_{OL} = 0.1$V

   Let $V_{t1} = V_{t2} = 1$ V and $V_{DD} = 5$ V, and neglect the body effect.

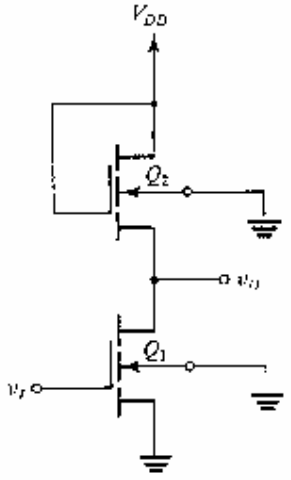

Fig.1

4. Use the approximate expressions (1) and (2) to determine t_P and DP for the inverter of problem (2). Let C = 0.1ρF

EMOS

Expression (1) : $t_P = 1/2\ t_{PLH} = 0.4C/\{K_2(V_{DD}-V_t)\}$

Expression (2) : $DP = 0.2CV_{DD}(V_{DD}-V_t)$