Alexandria Institute of Technology
Electronics Section

Course: Digital Integrated Circuits
Instructor: Prof. M. El-Banna

Sheet : 3
SAT and SUN

1- Use the expresion {DP = $0.2CV_{DD}(V_{DD}-V_t)$} to determine DP for an enhancement-load NMOS inverter operated from V_{DD} = 5V and having V_t = 1V. let C = 10 ρF.

2- A CMOS inverter in a VLSI circuit operating from a 5V supply has $(W/L)_n$ = 10μm/5μm, $(W/L)_p$ = 20μm/5μm , $\mu_n C_{OX} = 2\mu_p C_{OX} = 20\mu A/V^2$. If the total effective load capacitance is 0.1 pF find t_{PHL}, t_{PLH}, and t_P.

3- For the CMOS inverter {of exercise 2 in sheet 2}, which is intended for SSI and MSI circuit applications, find t_p if the load capacitance is 15 pF.

4- Calculate the delay-power product of the CMOS inverter of Exercise 2 when it is operating at a switching rate of 50 MHz.

CMOS

$t_{PHL} = 0.8C/K_nV_{DD} = 0.8C/2K_pV_{DD} = 0.4C/K_pV_{DD}$

$t_{PLH} = 0.8C/K_pV_{DD}$