COLLEGE OF ENGINEERING & TECHNOLOGY

Department: Electronics and Communications

Lecturer : Prof. Dr. Mohamed El-Banna **TA: Amr El-Helw**

Course : Electronic Circuits II

Course Code: EC 432 **Sheet 4**

1. The data sheet of the SN7400 quad 2-input NAND gate of TTL family provide the following:
   - Logic-1 input voltage required at both terminals to ensure a logic-0 level at the output : MIN (minimum) 2 V.
   - Logic-0 output voltage required at either input terminal to ensure a logic-1 level at the output: MAX (maximum) 0.8 V.
   - Logic-1 output voltage: MIN 2.4 V, TYP (typical) 3.3 V.
   - Logic-0 output voltage: TYP 0.22 V, MAX 0.4 V.
   - Logic-0-level supply current: TYP 12 mA, MAX 22 mA (for the entire package)
   - Logic-1-level supply current: TYP 4 mA, MAX 8 mA (for the entire package)
   - Propagation delay time to logic-0 level: TYP 7 ns, MAX 15 ns.
   - Propagation delay time to logic-1 level: TYP 11 ns, MAX 22 ns.

   a- Find the noise margin in both the 0 and 1 states.
   b- Assuming that the gate is in the 1 state 50% of the time and in the 0 state 50% of the time, find the average static power dissipated in a typical gate. The power supply voltage is +5 V.
   c- Assuming that the gate drives a capacitance C_L=45 pF and is switched at 1-MHz rate, find the dynamic power dissipation per gate using the typical values of the logic 1 and 0 levels at the output.
   d- Find the typical value of the gate delay-power product (neglecting the dynamic power dissipation)
2. A logic inverter having a negligible static power dissipation is switched at a rate of 1 MHz. If the inverter is operated from a 10-V power supply and drives a 50-pF load capacitance, find the dynamic power dissipation and the average current drawn from the power supply. Assume that the output levels are close yo 0 and 10 V.
3. An enhancement-load inverter having $(W/L)_1$=3 and $(W/L)_2$=1/3 is fabricated with a technology for which the minimum practical transistor dimension (length or width) is 5 μ m. Find the area occupied by this inverter and the value of its K_R. If K_R is to be quadrupled, find the ratio (W/L) for each device so that silicon area required by the inverter is the minimum possible.
4. Consider an enhancement-load inverter having V_{to}=1 V, $(W/L)_1$=3, $(W/L)_2$=1/3, $\mu_n c_{ox}$=20 μ A/V^2 , $2\varphi_f$ =0.6 V, γ =0.5V$^{1/2}$ and V_{DD}=5 V.

   a- Neglecting the body effect, find the critical points of the voltage transfer characteristic, and hence the noise margin.
   b- Taking the body effect into account, find the modified values of V_{OH} and NM_H.
   c- Find the inverter current in both states, and hence find the average static power dissipation.

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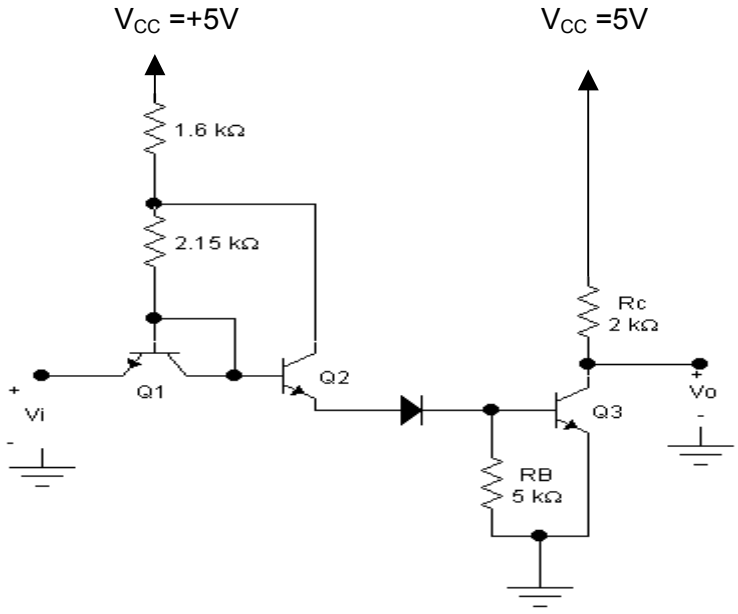
5. Consider the DTL gate circuit shown in the figure below and assume that $\beta\,(Q_2)=\beta\,(Q_3)=50$.

   a- When $v_I = 0.2$ V, find the input current.
   b- When $v_I = +5$ V, find the base current of Q_3.



6. The figure below shows the circuit that guarantees the reference voltage V_R. Assuming that the voltage drop across each of D_1 and D_2, and the base-emitter junction of Q_1 is 0.75V, calculate the value of V_R. Neglect the base current of Q_1.