Parallel Overloaded CDMA Interconnect (OCI) Bus Architecture for on-Chip Communication

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***Abstract*—On-chip interconnects are the performance bottleneck in modern System-on-Chips (SoCs). Bus topologies and Networks-on-Chip (NoCs) are the main approaches used to implement on-chip communication. The interconnect fabric enables resource sharing by Time and/or Space Division Multiple Access (T/SDMA) techniques. Code Division Multiple Access (CDMA) has been proposed to enable resource sharing in on-chip interconnects where each data bit is spread by a unique orthogonal spreading code of length N. Unlike T/SDMA, in wireless CDMA, the communication channel capacity can be increased by overcoming the Multiple Access Interference (MAI) problem. In response, we present two overload CDMA interconnect (OCI) bus architectures, namely TDMA-OCI (T-OCI) and Parallel-OCI (P-OCI) to increase the classical CDMA interconnect capacity. We implement and validate the T-OCI and P-OCI bus topologies on the Xilinx Artix-7 AC701 kit. We compare the basic SDMA, TDMA, and CDMA buses and evaluate the OCI buses in terms of the resource utilization and bus bandwidth. The results show that the T-OCI achieve 100% higher bus capacity, 31% less resource utilization compared to the conventional CDMA bus topology. The P-OCI bus provides N times higher bus bandwidth compared to the T-OCI bus at the expense of increased resource utilization.**

***Keywords*—SoC, CDMA, Bus Architecture, On-Chip Interconnect, CDMA Bus, Multiple Access Interference, Overloaded CDMA.**

I. Introduction

On chip communication profoundly impacts the overall area, performance and power consumption of modern gigantic System-on-Chips (SoCs). Increasing the communication overhead degrades the speedup achieved by parallel computing Developing efficient high-performance on-chip interconnects has been of paramount importance for the parallel and high-performance computing technologies. Buses and Networks-on-Chips (NoCs) are the most deployed interconnect topologies for interconnecting IP cores in SoCs [1]. Most interconnect topologies adopt either Time Division Multiple Access (TDMA) exemplified by time-shared multiplexers or Space Division Multiple Access (SDMA) exemplified by crossbars [2, Chapter 2,3]. Network-on-chips (NoCs) adopts a different on-chip interconnect paradigm based on packet switching instead of circuit switching adopted in bus topologies, though the basic switching elements of NoCs basically apply either TDMA or SDMA schemes in conjunction with buffering and storage devices to implement NoC routers and switches [3].

Code Division Multiple Access (CDMA) is another medium sharing technique that leverages code space to enable simultaneous medium access. In spread spectrum CDMA, multiple users simultaneously access the communication channel where each user is assigned a unique orthogonal spreading code to enable interference-free multiple access. CDMA has been proposed as an on-chip interconnect sharing technique for both bus and NoC interconnect architectures [4]. Many advantages of using CDMA for on-chip interconnect include reduced power consumption, fixed communication latency, and reduced system complexity [5]. The classical CDMA bus topology relies on the Walsh Hadamard orthogonal code family to enable bus sharing. Nikolic *et. al*. propose a full CDMA bus system in [6]. Bus wrappers convert address and data from IP cores into CDMA encoding while control signals are not encoded to facilitate interconnection to other TDMA buses [7].

Figure 1 shows the block diagram of the ordinary CDMA bus. The system is composed of a number of XOR encoders and accumulator-based decoders. In the encoder, an N-chip length Walsh spreading code is XORed with the data bit and sent out serially. The number of transmit-receive IP core pairs sharing the bus equals to M where $M \geq N-1$. Serial streams from all transmitting cores are added together and the binary sum is sent to a decoding circuit feeding the receiving IP cores. The decoding process is periodic and the decoding cycle lasts for N clock cycles. The despreading operation is realized by correlating the received sum with the spreading code assigned to the transmitter-receiver pair. Two accumulators are used to implement the correlation operation on the receiver side. The bus data is passed to the zero accumulator when the current chip value equals to "0" and to the one accumulator when the chip value equals to "1", which is equivalent to multiplication by ± 1. At the end of the decoding cycle, the difference between the two accumulators is always $\pm N/2$ (the auto correlation result) and the sign indicates encoded data [8].

Multiple Access Interference (MAI) sets an upper bound on the CDMA system capacity. By overcoming the MAI problem, the CDMA interconnect capacity can be significantly increased without degrading the interconnect performance or increasing resource utilization. CDMA channel overloading is a known technique used in wireless communications to increase the communication channel capacity [9]. As an on-chip interconnect topology, our main objective is increasing the number of elements sharing the ordinary CDMA bus while keeping the system complexity unchanged by using simple encoding circuitry and relying on the accumulator-based decoder with minimal changes. In our previous work, we presented the MAI-Overloaded CDMA Interconnect (M-OCI) bus topology which increases the bus capacity by 25% [8]. In this work we advance the TDMA OCI (T-OCI) and Parallel-OCI (P-OCI) topologies to increase the bus capacity by 100%. Code overloading for both topologies relies on exploiting special properties of the used spreading code set, namely Walsh Hadamard code family, to add a set of identifiable non-orthogonal spreading codes.

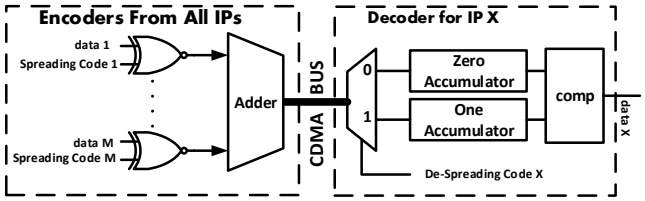


Fig. 1. Ordinary CDMA Bus Topology

The remaining of this paper is organized as follows: Fundamentals and mathematical foundations of the T-OCI and P-OCI code design are presented in Section II. Implementation details of the OCI bus topologies is presented in Section III. Performance evaluation of the OCI bus topologies in terms of resources and bus bandwidth is presented in Section IV. Conclusions and future work are portrayed in Section V.

II. Overloaded CDMA Interconnect (OCI) Code Design

In this section, we will provide the the code design methodology, mathematical foundations, and decoding details of the proposed OCI codes. The Walsh Hadamard spreading code family has a featured property that enables OCI code design. The difference between any consecutive channel sums of data spread by the orthogonal spreading codes is always even for an odd number of transmit-receive pairs M regardless of the spread data. This property means that for the $N-1$ transmit-receive pairs using the Walsh orthogonal codes, one can encode additional $N-1$ data bits in consecutive differences between the N chips of the spreading code. Thus, exploiting this property enables adding %100 non-orthogonal spreading codes which doubles the CDMA bus capacity. Unlike the ordinary CDMA XOR encoder, an AND gate is used to encode data with non-orthogonal spreading codes. For each non-orthogonal encoder, a single spreading chip summoned at a specific time slot is added to the bus sum if the transmitted data is "1" which causes the consecutive sum difference to deviate. Because the proposed codes are identical to TDMA signals we call this code family T-OCI codes. Therefore the developed bus architecture is called TDMA Overloaded on CDMA Interconnect or simply T-OCI. Unfolding the serial transmission of the CDMA bus enables all the encoded data to be transmitted in parallel, thus improving the bus bandwidth N times. Hence, we also propose the P-OCI bus which is the unfolded version of the T-OCI. In the P-OCI bus, the encoder adder circuitry are replicated N times to allow the transmission of the the encoded data in one clock cycle.

The bus sum equation for the T-OCI codes is written as:

$$Bus_{sum} = \sum_{j=1}^{N-1} (-1)^{d_C(j)} C_o(j) + \sum_{j=N+1}^{2N-1} d_T(j).T(j-N+1) \quad (1)$$

where Bus_{sum} is the N-cycle waveform of the bus sum, $d_C(j)$ is the orthogonal CDMA data bit sent by the j^{th} user and $d_T(j)$ is the non-orthogonal TDMA data bit sent by the j^{th}, and $C_o(j)$ is the orthogonal code assigned to the j^{th} user, $T(j-N+1)$ is the TDMA code assigned to the j^{th} user. The TDMA code $T(i)$ is a single chip or a rectangular pulse assigned at time i. The TDMA part of the bus sum equation can be viewed as an additional N-chip spreading code that cause MAI to the first part of the equation representing the sum of orthogonal spread data. It should be indicated that the first chip of the TDMA MAI code is always zero ($T(1)=0$), and the remaining $N-1$ chips are determined by the encoded binary data. Equation 1 can be rewritten as:

$$Bus_{sum} = \sum_{j=1}^{N-1} (-1)^{d_C(j)} C_o(j) + C_n(d_T) \quad (2)$$

where $C_n(d_T)$ is the TDMA MAI code as a function of the non-orthogonal data spread.

Despreading of the k^{th} orthogonal receiver is achieved by multiplying the bus sum by the k^{th} orthogonal spreading code $C_o(k)$. Equation 3 gives the the orthogonal receiver output.

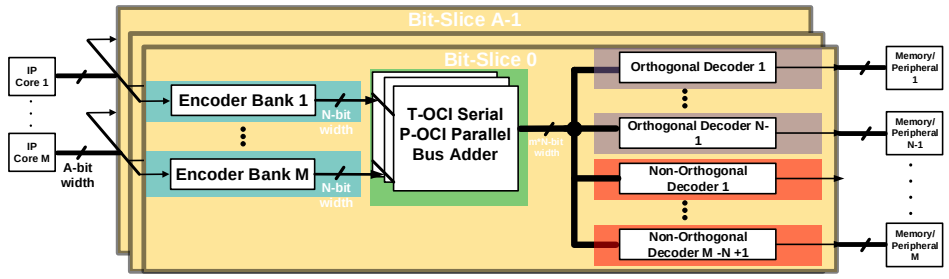
$$corr_{dec}(k) = (-1)^{d_C(j)} N/2 + C_o(k).C_n(d_T) \quad (3)$$

The first term of the equation represents the auto correlation term which is equal to $\pm N/2$ according to the data spread d_C. The second term of the equation represents the MAI added by the TDMA codes. The maximum MAI value contributed by the second term is $\pm N/2$ This case of maximum MAI can only occur if the MAI TDMA code constructed by the non-orthogonal encoded data is identical to $C_o(k)$ or its complement $\overline{C_o(k)}$ which yields $\pm N/2$, respectively.

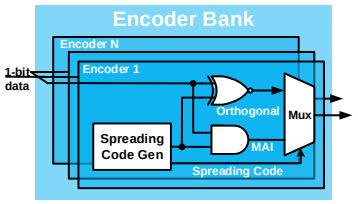
As long as the MAI magnitude $|C_o(k).C_n(d_T)| < N/2$, the non-zero correlation result will always facilitate correct decoding of orthogonal data where the comparator circuit can still be used to detect the accumulator sign. The main challenge is decoding orthogonal data when the MAI TDMA code is identical to the spreading code or its complement which might cause the correlation result to be zero. Zero correlation indicates either cases of ($d_C = 0$ and $C_n(d_T) = \overline{C_o(k)}$) or ($d_C = 1$ and $C_n(d_T) = C_o(k)$). However, because we forced the first chip of the MAI TDMA code $C_n(d_T)$ to be always zero we can exclude the first case because all Walsh orthogonal spreading codes start with "0". Therefore, the zero correlation result always indicates that the orthogonal data encoded is "1". Decoding the non-orthogonal TDMA data can be achieved by exploiting the even difference property of the Walsh orthogonal codes. As we are only interested in even or odd check of the difference between consecutive sums on the bus, a two-input XOR gate is used. The XOR gate inputs are the LSBs of the two bus sums corresponding to the first chip in the spreading code and to the chip where the TDMA MAI is added.

III. Overloaded CDMA Interconnect (OCI) Bus Architecture

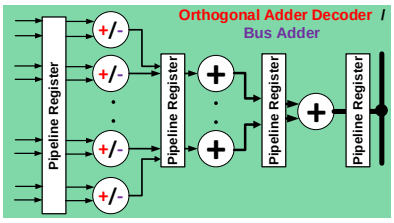
We implemented two variants of the T-OCI and P-OCI buses, a reference architecture and a pipelined architecture. The OCI bus architecture shown in Figure 2(a) is basically composed of three parts: the encoder wrappers, the decoder wrappers and the bus adder. The encoder is hybrid, it can encode both orthogonal and non-orthogonal data. The data is XORed and ANDed with the orthogonal and non-orthogonal spreading code, respectively, and a multiplexer chooses only one output according to the code assigned dynamically as depicted by Figure 2(b). Only one encoder is required to encode one data bit in the T-OCI, but N encoders are required for the P-OCI since the code must be modulated in parallel. For a spreading code of length N, the number of



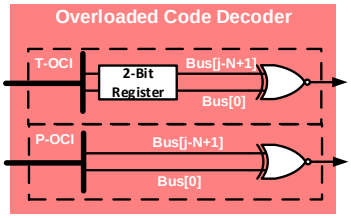
(a) OCI Bus architecture



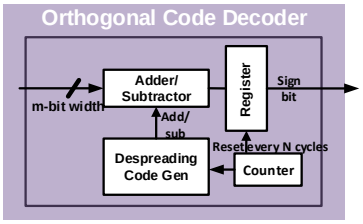
(b) Hybrid encoder



(c) Pipelined tree adder serving as a bus adder or a P-OCI orthogonal code decoder



(d) Overloaded spreading code decoder in T-OCI or P-OCI buses



(e) Orthogonal spreading code decoder in conventinal CDMA and T-OCI buses

Fig. 2. Pipelined OCI bus high-level architecture and bus components of the conventional, T-OCI and P-OCI bus variants

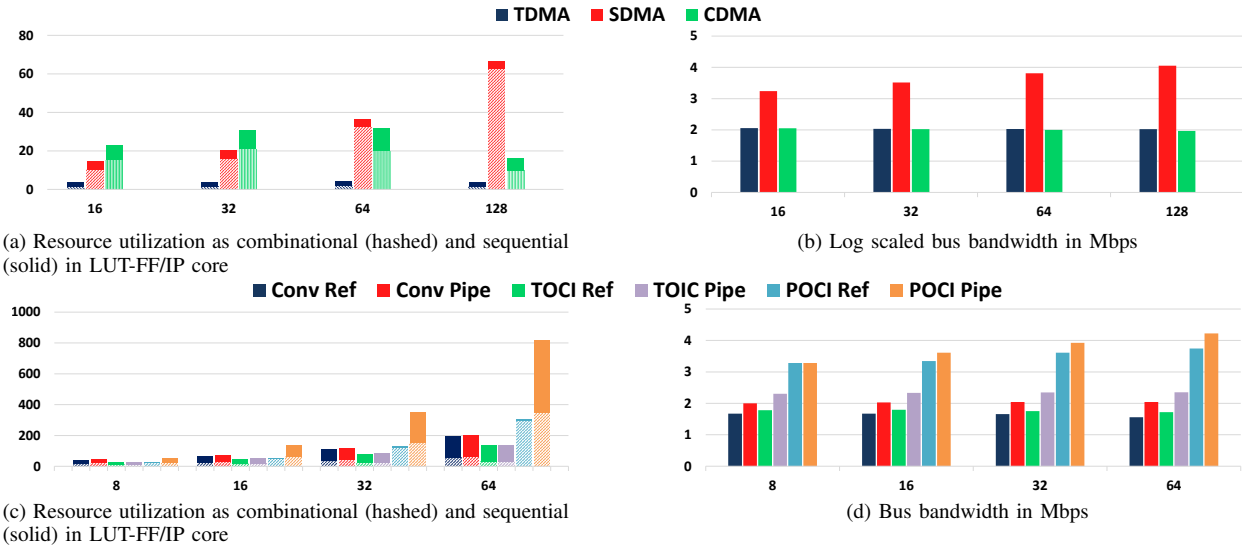
transmit-receive element pairs M is equal to $2(N-1)$. In the T-OCI architecture, the bus adder is a tree adder of M inputs, ($\lceil \log_2 M \rceil = \log_2 N + 1$) stages, and m-bit output width where ($m = \lceil \log_2 M \rceil$) as shown by Figure 2(c). In the pipelined architecture, ($\lceil \log_2 M \rceil$) stages of pipelining registers are inserted after each level of the tree. For the P-OCI architecture, the bus adder is replicated N times to enable all the N spreading chips of all users to be transmitted in parallel.

There are three decoder types for different OCI buses: the orthogonal despreading accumulator, orthogonal despreading adder, and overloaded code decoders. The orthogonal despreading accumulator decoder is an accumulator implementation of the correlator receiver. $N-1$ accumulator decoders are instantiated in the T-OCI bus for orthogonal data despreading. In the T-OCI architecture, instead of using two accumulators, we implemented an up-down accumulator whose accumulated result is the difference between what used to be the two accumulators as shown in Figure 2(e). In the P-OCI architecture, the despreading accumulator is implemented as an adder to directly add all the received bus data as depicted in Figure 2(c). In the first stage of the adder decoder, all the bus values corresponding to a zero despreading chip are subtracted from those corresponding to a one despreading chip, which represents multiplying the bus sum by the despreading code, and the results are then added at the subsequent stages. The overloaded code decoder depicted in Figure 2(d) is a simple XOR gate. In the T-OCI bus, a 2-bit register is used to store the Least-Significant Bit (LSB) of two bus values, first of which is the $Bus_{sum}(0)$ and the second is $Bus_{sum}(j-N+1)$, where j is the number of the T-OCI decoders ($N \leq j \leq 2N-2$). In the P-OCI bus, there is no need for this register since the XOR gate can take its inputs directly from the parallel bus.

IV. Performance Evaluation

In this section we present the performance evaluation results of the developed OCI buses. To evaluate the CDMA bus performance relative to the TDMA and SDMA buses, we implemented the basic bus architectures for the three sharing techniques. For an $M \times M$ interconnect, the TDMA bus is simply implemented as an $M \times 1$ multiplexer while the SDMA bus is implemented as M multiplexers each $M \times 1$ back-to-back connected to M demultiplexers each $1 \times M$, and the bus arbitration and control circuitry are not implemented. All bus architectures are implemented on the Xilinx Artix-7 AC701 kit and the synthesis results are illustrated in Figure 3. The resource utilization is expressed as the number of LUTs and FFs and normalized to the number of interconnected transmit-receive pairs M. As depicted in Figure 3(a),the resources utilized per element in case of the TDMA bus is constant $\approx M/M \approx 1$. For SDMA, the utilization per element $\approx M^2/M = M$ which is a near linear trend as shown in Figure 3(a). The CDMA resource utilization per element $\approx Mlog_2(M)/M$ which results in a logarithmic utilization trend. The SDMA bus bandwidth, on the other hand, is M-folds the constant bandwidth of the SDMA and CDMA buses which is depicted by the log-scaled bandwidth comparison of Figure 3c(b). This analysis shows that the conventional CDMA bus has a higher area set-back when compared to the TDMA bus but offers equal bandwidth. Also the conventional CDMA bus has lower bandwidth set-back against the SDMA bus but much smaller area. The OCI bus architectures thus offer a trade-off between the two set-backs by bandwidth improvement and area per element reduction.

The resource utilization expressed in LUTs and FFs per IP core and the bandwidth of the conventional CDMA, T-OCI, and P-OCI buses are illustrated in Figure 3, each bus has the reference and pipelined architecture variants. A full capacity bus was implemented, i.e. the number of IP cores is the maximum number offered by the bus. All CDMA bus variants are implemented and validated on an Artix-7 AC701 FPGA kit. We compare the developed buses for different spreading code lengths $N = \{8, 16, 32, 64\}$. To establish a fair comparison between different bus architectures, the performance metrics for a bus interconnecting M transmit-receive pairs are divided by M to evaluate bus performance per element. As depicted by Figure 3(c), for a fixed spreading code of length N, resource utilization per IP core of the T-OCI bus is less than the



(a) Resource utilization as combinational (hashed) and sequential (solid) in LUT-FF/IP core

(b) Log scaled bus bandwidth in Mbps

(c) Resource utilization as combinational (hashed) and sequential (solid) in LUT-FF/IP core

(d) Bus bandwidth in Mbps

Fig. 3. Synthesis and implementation results of the basic S/T/CDMA and OCI buses for spreading code length $N = \{8, 16, 32, 64\}$.

conventional CDMA bus by 31% due to the significant increase in bus capacity compared to the marginal overhead added by the bus circuitry. The P-OCI bus, however, is 400% larger than the conventional bus due to the parallel bus adders. Increasing N increases the resource utilization due to the increased bus complexity. More specifically, with increasing N, the size of the bus adder and the decoder circuitry increases.

For all reference architectures, the operating frequency is limited by the critical path length of the bus adder. The pipelined architecture splits the adders' critical path into $\lceil log_2(N) \rceil + 1$ stages, which improves the maximum bus frequency at the expense of the extra non-architectural registers and output latency. With increasing N, the drop in the maximum bus frequency is compensated by the increase in the bus bandwidth due to the capacity enhancement offered by the OCI buses as shown by Figure 3(d). For a fixed N, we can see the enhancement of the bus bandwidth for the T-OCI and P-OCI buses over the ordinary CDMA buse. Generally, the CDMA bus bandwidth BW is given by the following equation:

$$BW = \frac{N_{bits} * f_b * M * R}{N} \tag{4}$$

where N_{bits} is the number of interconnected bits per IP core (data bus width), f_b is the bus frequency and R is the number of replicas of the bus adder. The T-OCI bandwidth has significant improvement over the ordinary CDMA bus as it has an overloading ratio of $\frac{M}{N} = 2$, compared to the basic CDMA bus ratio of $\frac{M}{N} = 1$. $R = 1$ for both the conventional and T-OCI buses, however, for the P-OCI bus, $R = N$. Therefore the P-OCI bus offers $2N$ times the bandwidth of the conventional CDMA bus at the expense of the resource utilization.

V. Conclusions

In this work, we presented the T-OCI bus that leverages the overloaded CDMA concept to increase the CDMA bus capacity by 100%. We also present the P-OCI bus which is a higher bandwidth alternative of the T-OCI bus at the expense of higher resource utilization. The OCI architectures can replace the T/SDMA topologies to implement on-chip interconnects in either bus or NoC topologies. The T-OCI and P-OCI bus topologies were implemented and validated on Artix-7 AC701 FPGA kit. We compared the OCI buses performance with the conventional CDMA bus normalized to the number of interconnected transmit-receive pairs. When compared to the conventional CDMA bus, the T-OCI bus achieves 100% higher bandwidth over the conventional bus while the P-OCI bus achieves $N \times 100\%$ more bandwidth, where N is the spreading code length. The T-OCI buse utilizes 31% more resources than the conventional CDMA bus, while the P-OCI requires 400% more resources . Many directions for the future work are inspired by this research including: finding more non-orthogonal codes to increase the bus capacity, exploring more architectural optimizations to the proposed bus topology, and investigating the OCI application to NoC interconnects.

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