A Standalone Burst-Mode Receiver With Clock and Data Recovery, Clock Phase Alignment, and RS(255, 239) Codes for SAC-OCDMA Applications

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***Abstract*—We demonstrate a standalone (no global clock) burst-mode receiver (BMRx) for a 7 $\times$ 622 Mb/s incoherent spectral-amplitude-coded optical code-division multiple-access system. The receiver provides the following functions: quantization (intensity noise filtering), clock and data recovery, burst-mode functionality (automatic phase acquisition) using a clock phase aligner (CPA), framing (for byte synchronization), and forward-error correction (FEC) using a (255, 239) Reed–Solomon decoder. The receiver provides an instantaneous (zero preamble bit) phase acquisition time for any phase step ($\pm 2\pi$ rads) between consecutive packets. With the CPA, we report a zero packet loss ratio (PLR) for up to four simultaneous users and more than a 300-fold improvement in the PLR for a fully loaded system. The BMRx also accomplishes more than 2.5 dB of coding gain, and achieves error-free (bit-error rate $< 10^{-9}$) operation for a fully loaded system.**

***Index Terms*—Burst-mode receiver (BMRx), clock and data recovery (CDR), clock phase aligner (CPA), forward-error correction (FEC), spectral-amplitude-coded optical code-division multiple-access (SAC-OCDMA).**

I. Introduction

SPECTRAL-AMPLITUDE-CODED optical code-division multiple-access (SAC-OCDMA) is a good candidate for optical multiaccess networks over other OCDMA techniques because of its ability to cancel multiple access interference (MAI), and to permit the use of low-speed electronics operating at the bit rate [1], [2]. Furthermore, advances in writing fiber Bragg gratings (FBGs) enable the design of low cost and compact passive encoders/decoders well adapted to passive optical networks (PONs) [2]. Much research into OCDMA focuses on optical design, while assuming the availability of high-speed electronics [1], [2]. Emerging research is concerned with the electronic design of receivers for optical multiaccess networks, featuring postprocessing functionalities [3], [4]. Previous electronic receivers were reported in the literature for fast-frequency hop (FFH) OCDMA and PON systems [5], [6].

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FFH-OCDMA and SAC-OCDMA have distinctive detection strategies. FFH-OCDMA (or $\lambda - t$ OCDMA) requires electronics that operate at the chip rate rather than the data rate to exploit the time-domain processing gain. SAC-OCDMA enjoys excellent MAI rejection with balanced detection, and the advantage of operating at the data rate, thus enabling higher bit rates for fixed electronic processing speeds. However, the asynchronous nature of the OCDMA system, introduces random phase steps $\Delta\varphi$ between consecutive packets, making the data bursty in nature. In this letter, we demonstrate experimentally for the first time, to our knowledge, an OCDMA system tested in a bursty environment. More specifically, we demonstrate an incoherent SAC-OCDMA system supporting seven asynchronous users at 622 Mb/s (FFH results were for six users at 155 Mb/s) with no global clock, that is, using a standalone burst-mode receiver (BMRx). The BMRx includes a quantizer to filter intensity noise, clock and data recovery (CDR), a clock phase aligner (CPA) to instantaneously account for phase variations of $\pm 2\pi$ rads between consecutive packets (not demonstrated in [5]), and a forward-error correction (FEC) module with (255, 239) Reed–Solomon (RS) codes. We quantify the increase in soft capacity via FEC, while working with a nonideal recovered clock that provides realistic, achievable sampling.

II. SAC-OCDMA System Architecture

The SAC-OCDMA test bed is presented in Fig. 1. A shared incoherent broadband source is filtered around 1542.5 nm using two cascaded FBG bandpass filters providing a 9.6-nm band. The light is then modulated with a nonreturn-to-zero (NRZ) $2^{15}-1$ pseudorandom binary sequence (PRBS) using a polarization-independent electroabsorption modulator. The desired information rate per user is 622 Mb/s. As the RS(255, 239) code introduces ~15/14 of overhead, we used an aggregate bit rate of 666.43 Mb/s. The modulated signal is spectrally encoded using seven FBGs (corresponding to seven users) working in transmission; balanced incomplete block design codes with length 7 and weight 3 are used as user signature codes as in [2]. After encoding, signals from different users are delayed differently with random optical delay lines to decorrelate the data, and combined on a single fiber. At the receiver side, a variable optical attenuator is used to control the received power. Two FBGs, also working in transmission, are used to decode the desired user prior to balanced photodetection [2]. The output of the balanced photodetector is then amplified and low-pass filtered by

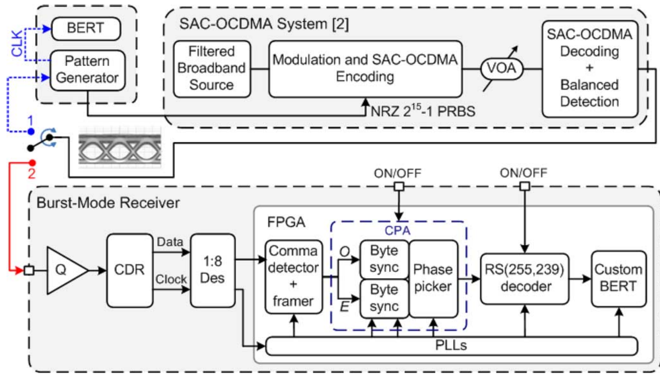

Fig. 1. Block diagram of 7×622 Mb/s SAC-OCDMA experimental setup with the BMRx. PLL: phase-locked loop.

a fourth-order Bessel–Thomson filter whose -3-dB cutoff frequency is 0.7 $\times$ bit rate, or 467 MHz. Such a filter reduces intensity noise from the broadband source, while keeping intersymbol interference to a minimum [7]. Bit-error-rate (BER) measurements are then performed with either a global clock, or through our OCDMA BMRx, corresponding to switch position "1" or "2", respectively. To generate alternating packets with adjustable phase, packets from two programmable ports (not shown in Fig. 1) of the pattern generator are concatenated via a power combiner and used to drive the modulator [4]. These packets are formed from preamble bits, delimeter bits, a payload, and comma bits. A phase step and a silence period consisting of an all-zero sequence whose length is equal to the tested number of consecutive identical digits is inserted between packets. The phase steps between packets can be set ± 2 ns with 2-ps resolution, corresponding to a ± 1.25 unit interval (UI) at 622 Mb/s. Note that 1 UI corresponds to a bit period.

III. SAC-OCDMA Receiver

The SAC-OCDMA receiver we designed is shown in Fig. 1. Our receiver without the CPA is, therefore, similar to that in [5], but simpler because it does not need a return-to-zero (RZ)-to-NRZ converter as required for FFH-OCDMA. The quantizer (Q) is used to apply a certain threshold to the incoming signal in order to filter out intensity noise. The threshold was manually adjusted to sample in the middle of the eye opening, to obtain the optimum BER. The CDR recovers the clock and the data from the incoming signal. The multirate CDR is from Analog Devices (ADN2819) and supports the following frequencies of interest: 622 Mb/s (without FEC), 666.43 Mb/s (with FEC), and 1.25 Gb/s for burst-mode operation at $2\times$ the bit rate. The CDR is followed by a 1 : 8 deserializer from Maxim-IC (MAX3885). The deserializer parallelizes the data to reduce the frequency of the recovered clock and data to a frequency that can be processed by the digital logic. The parallel data and the divided clock are then brought onto a Virtex II Pro FPGA from Xilinx for further processing.

On the FPGA, automatic detection of the payload is implemented through a framer and a comma detector that are responsible for detecting the beginning (delimeter bits) and the end (comma bits) of the packet, respectively [5]. The CPA makes use of a phase picking algorithm [4] and the CDR operated in $2\times$ oversampling mode. The CPA is turned on for the packet loss ratio (PLR) measurements with phase acquistion, otherwise it is bypassed. The idea behind the CPA is based on a simple, fast, and effective algorithm. The odd and the even samples resulting from sampling the data twice on the alternate (odd and even) clock rising edges, are forwarded to path O and to path E, respectively. The byte synchronizer is responsible for detecting the delimiter. It makes use of a payload detection algorithm to look for a preprogrammed delimeter. The idea behind the phase picking algorithm is to replicate the byte synchronizer twice in an attempt to detect the delimiter on either the odd and/or even samples of the data, respectively. That is, regardless of any phase step, $|\Delta\varphi| \leq 2\pi$, between two consecutive packets, there will be at least one clock (odd or even) edge that will sample either of the data samples correctly. The phase picker then uses feedback from the byte synchronizers to select the right path. Note that a phase step of $\pm\pi$ rads corresponds to ± 800 ps at $\sim$622 Mb/s.

The realigned data is then sent to the RS(255, 239) decoder which is turned on for the BER measurements with FEC, otherwise it is by-passed. The RS decoder is an IP core from Xilinx LogiCORE portfolio. The FPGA-based BER tester (BERT) is implemented to selectively perform BER and PLR measurements on the payload of the packets. This eliminates the need to up convert the frequency back to 622 Mb/s or 666.43 Mb/s using an 8 : 1 serializer after the FPGA. Also, the phase step response of the burst-mode CDR can make a conventional BERT lose pattern synchronization at the beginning of every packet. Using the custom BERT, synchronization is instantaneous at the beginning of every packet, therefore enabling measurements on noncontinuous, bursty data, overcoming the limitations of BERTs which require continuous synchronization.

IV. Results and Discussion

The BER performance of the SAC-OCDMA system for one, three, five, and seven simultaneous users is shown in Fig. 2. The horizontal axis represents the useful power, the received power from the desired user. Focusing on the set of curves for the global clock and for the recovered clock, we note that error-free transmission (BER $< 10^{-9}$) is achieved only for up to five simultaneous users. A BER floor at $\sim 10^{-6}$ is reached for seven users because of the intensity noise added by the MAI as seen from the eye diagrams [7]. It can also be inferred that a negligible penalty (less than 0.25 dB at BER $= 10^{-9}$) is added due to the nonideal sampling of the CDR. Note, at power levels smaller than -26 dBm, we were able to accurately control manually the decision threshold (using a dc power supply) for the CDR measurements, compared to the use of the automated decision threshold in the BERT for global clock measurements. The manual optimization explains the slight improvement in the performance when using the recovered clock at lower power levels. Eye diagrams measured at -18 dBm are included as insets in Fig. 2. The single-user eye diagram is a very open eye, while the fully loaded system with seven users has a severely closed eye. Despite the eye closure for seven users, the FEC allows us to return to the waterfall curve similar to that of the single-user case. Specifically, error-free transmission (BER $< 10^{-9}$) is achieved for all seven users. A coding gain of more than 2.5, 2.7, and 5 dB

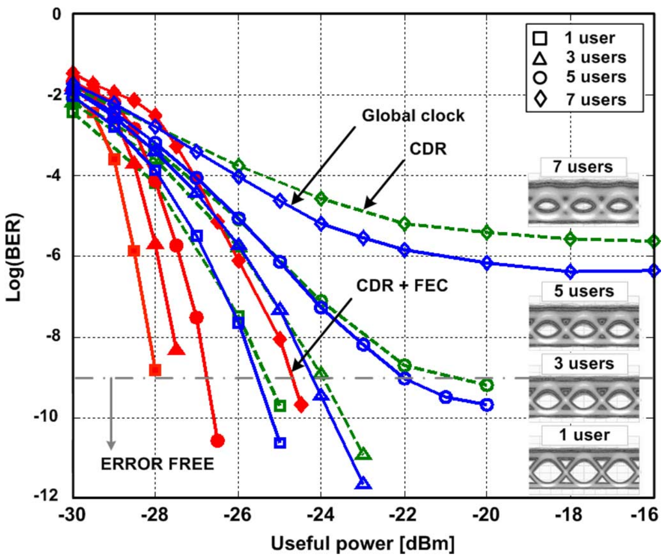

Fig. 2. BER performance for the SAC-OCDMA system. Dashed curves for global clock; solid curves and unfilled markers for recovered clock; and solid lines and filled markers for recovered clock with FEC.

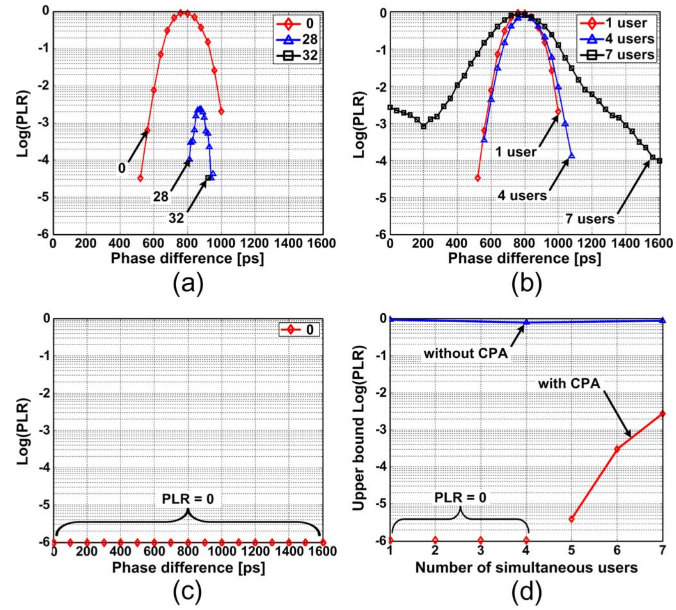

Fig. 3. PLR performance of the SAC-OCDMA system. (a) With CDR at 622 Mb/s for a single user with different preamble lengths. (b) Effect of increasing number of simultaneous users with a zero preamble. (c) With CPA for a zero preamble. (d) Worst-case PLR comparison with and without CPA.

(measured at $\mathrm{BER} = 10^{-9}$) for one-, three-, and five-user cases, respectively, is achieved. Furthermore, the BER floor for seven users is eliminated.

Fig. 3 shows the PLR performance of the SAC-OCDMA system.[1] The PLR versus phase step for a single user with only the CDR (without the CPA), is depicted in Fig. 3(a) for different preamble length: 0, 28, and 32. The reason why we have bell-shape curves centered at 800 ps is that this represents the half bit period corresponding to the worst-case phase step at π rads, and therefore, the CDR is sampling exactly at the edge of the eye diagram. Preamble bits ("1010..." pattern) can be inserted at the beginning of the packet to help the CDR settle down and acquire lock. As the preamble length is increased, there is an improvement in the PLR. After 32 preamble bits, we observe a zero PLR for any phase step. However, the use of a preamble reduces the effective throughput and increases delay. Fig. 3(c) shows the PLR versus phase step when the CPAis turned on. We observe zero PLR for any phase step between the packets with a zero preamble length giving instantaneous phase acquisition. Fig. 3(b) shows the effect of increasing the number of simultaneous users (for a zero preamble and without CPA). As the number of users is increased, the PLR at a particular phase step becomes worse. With the CPA turned on, for up to four simultaneous users, we observe instantaneous phase acquisition for any phase step, giving the same plot as in Fig. 3(c). However, for more than four users, with the CPA, the PLR tends to deteriorate as shown in Fig. 3(d), due to the severe eye degradation caused by MAI intensity noise. Here, we also compare the worst-case PLR versus number of simultaneous users with and without the CPA. We can finally extract from the figure that in case of a fully loaded system and despite the nonideal sampling of the CDR, the CPA can improve the performance by two orders of magnitude.

[1]All the PLR plots are shown from $0 \leq \Delta\varphi \leq 2\pi$ rads. However, the curves are symmetrical about 0 rads from $-2\pi \leq \Delta\varphi \leq 0$ as well.

V. Conclusion

We demonstrated a standalone BMRx for a 7×622 Mb/s incoherent SAC-OCDMA system. To our knowledge, this is the first time that an OCDMA system has been tested in a bursty environment. The receiver features automatic detection of payload, CDR, instantaneous (zero preamble bit) phase acquisition for any phase step ($\pm 2\pi$ rads) between consecutive packets, and FEC. The effect of intensity noise and other impairments was significantly reduced. The BER penalty was low when using the recovered clock instead of the global clock. Error-free transmission was achieved for a fully loaded system; coding gain of more than 2.5 dB was measured. With the CPA, we measured a zero PLR for up to four simultaneous users and more than a 300-fold PLR improvement for a fully loaded system.

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